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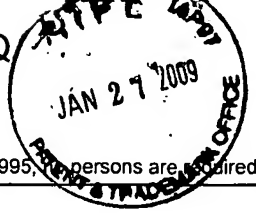

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
JRL-550-477

Application Number	Filed
10/714,178	November 17, 2003
First Named Inventor: ORION	
Art Unit: 2136	Examiner: Daniel L. HOANG.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1.34 _____

Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

January 27, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

ELWOOD et al.

Atty. Ref.: 550-655; Confirmation No. 8029

Appl. No. 11/095,655

TC/A.U. 2183

Filed: April 1, 2005

Examiner: Vicary, Keith E.

For: CONDITION BRANCH INSTRUCTION ENCODING WITHIN A MULTIPLE INSTRUCTION SET DATA PROCESSING SYSTEM

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January 27, 2009

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Clear Error #1: Gonzales and Alverson Fail to Teach All the Independent Claim Features

Claims 1-7 and 10-17 stand rejected as allegedly being obvious in view of Gonzales (US 5,488,688)and newly-applied Alverson (US 7,020,767). This rejection is respectfully traversed.

Gonzales describes a trace function that can operate in two modes. In the first mode, which is known as normal diagnostic mode, the trace function and the CPU are linked together so that the CPU is halted whenever the trace function (i.e., the FIFO) is halted. The trace function is halted in response to an event condition. A user can then examine the contents of the FIFO to determine the flow of software instructions that were executed prior to the event. In the second mode, called a FIFO halt mode, the CPU is not halted when the FIFO is halted to enable real time debug of the CPU. The second mode is used with debugging systems that require real time functionality, e.g., debugging a Hard Disk Drive controller. While the trace function is stopped to allow the debugger to access information from the FIFO, the CPU keeps on running its application. Halting the FIFO could be viewed as "suppressing the capture of diagnostic

data." Whether the FIFO is halted and the CPU continues to run depends on bits in the control register of the controller. See col. 4, lines 30 – 38 and Table IV. The FIFO may also be halted in response to an event condition. Event conditions are listed in Table II. These conditions are all linked to usual requests (breakpoints, external debug request, trace request). But none is linked to the domain in which the processor is operating. Furthermore, the capturing of diagnostic data is simply stopped in Gonzales by halting the FIFO, it is not suppressed in one domain while being allowed in another.

The combination of Gonzales and Alverson, even if it could be made for purposes of argument, fails to disclose or suggest "control logic configured to control said monitoring logic in dependence on said at least one control parameter and the domain in which said processor is operating to suppress capturing of diagnostic data relating to predetermined activities of said processor in said first domain while allowing capturing of diagnostic data relating to predetermined activities of said processor in said second domain," as recited in claim 1.

The Examiner now admits that Gonzales lacks (1) a processor that operates in two different domains and (2) a teaching "that while diagnostic data capture is being suppressed in one domain, capturing of diagnostic data in the second domain is allowed." See page 3. Although the Examiner cites Alverson for missing feature number (1), the Examiner also admits that neither Gonzales nor Alverson discloses missing feature (2). Nevertheless, the Examiner alleges that Alverson's teaching that "two events can be performed simultaneously within one processor" is analogous to "allowing capture of diagnostic data in one domain while suppressing it in another."

The analogy is faulty. Processing two events simultaneously on one processor simply means that two different programs are executed in parallel. Such a processor is sometimes referred to as a multi-threaded processor. But there is no teaching in Alverson of capturing of

diagnostic data or suppressing capture of diagnostic date. A person of ordinary skill in the data processing art would not have understood executing two programs in parallel to be the same as "allowing capture of diagnostic data in one domain while suppressing it in another." This faulty analogy is not a valid substitute for prior art evidence that actually teaches the admitted missing feature of "allowing capture of diagnostic data in one domain while suppressing it in another."

In contrast to Gonzales and Alverson, the claimed technology stops the monitoring logic from capturing data relating to the activities of the processor, when the processor is operating in a given domain. Such a domain may be for example a secure domain, or any domain where it is wanted to prevent activity of the processor to be monitored by an external debugger. The condition to suppress the capturing of data is hence related to the domain the processor is running in, and not just to usual debug events as in Gonzales. The monitoring logic is selectively prevented from capturing data relating to the activities of the processor when the processor is operating in a given domain. Such a domain may be for example a secure domain or any domain where it is desirable to prevent activity of the processor to be monitored by an external debugger. The condition to suppress the capturing of data is hence related to the **domain** the processor is running in--and not just to usual debug events as in Gonzales.

The claimed technology addresses and solves the problem of leakage of data between domains during diagnostic monitoring, and thus, allows granularity of the monitoring by enabling suppression of the capture of data in one domain while allowing it in another. Gonzales and Alverson are not concerned with this data leakage problem between domains. Instead, Gonzales allows trace data to be output from a processor while the CPU is still functioning. Alverson's goal is even more remote, i.e., to allow a multithreaded processor to detect and process events without interrupt notifications (see col. 7, lines 18-30).

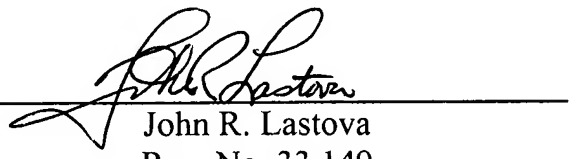
Claim 1 also recites "a storage element configured to store at least one control parameter." The Examiner refers to col. 3, lines 29 – 32 of Gonzales for this feature. This text describes a SERIAL I/O signal that is received by the controller, but it does not disclose that the SERIAL I/O signal is stored in a storage element. Instead, the SERIAL I/O signal directs the controller to either halt the CPU and the FIFO or just halt the FIFO depending on the signals received. Thus, this section does not disclose a storage element for storing the claimed control parameter.

Clear Error #2: Gonzales Fails to Teach All the Independent Claim Features

The Examiner maintains the rejection of claims 2 and 11 based on Gonzales. The Examiner equates the normal diagnostic mode (CPU and FIFO halted) in Gonzales as the claimed non-secure mode and the FIFO halt mode (FIFO halted and CPU running) in Gonzales as the claimed secure mode. But there is no indication of what the Examiner considers to be the secure domain and the non-secure domain in Gonzales. In fact, the claimed domains are not disclosed in Gonzales, as admitted by the Examiner on page 3 of the final rejection.

The final rejection is improper and should be withdrawn. Accordingly, the application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,
NIXON & VANDERHYE P.C.

By: 
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